GaN HEMT器件的研究现状、特点及应用

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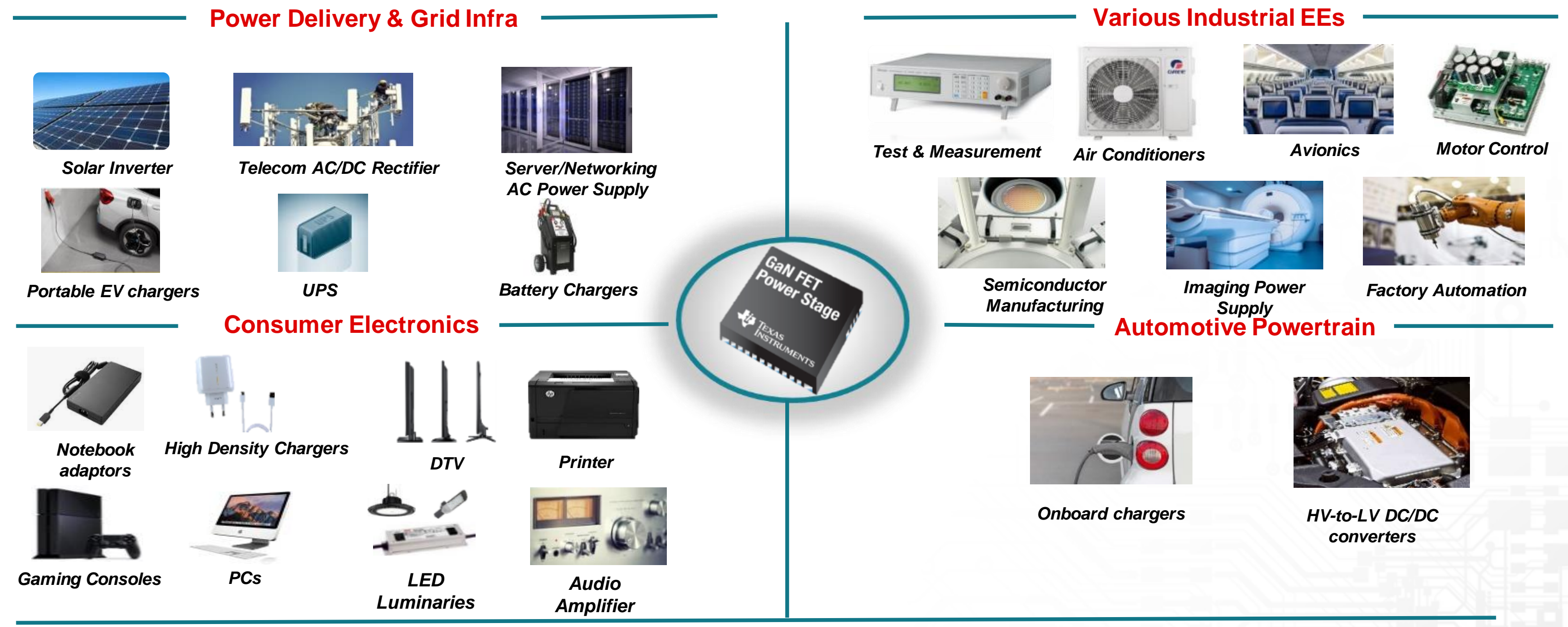
Agenda

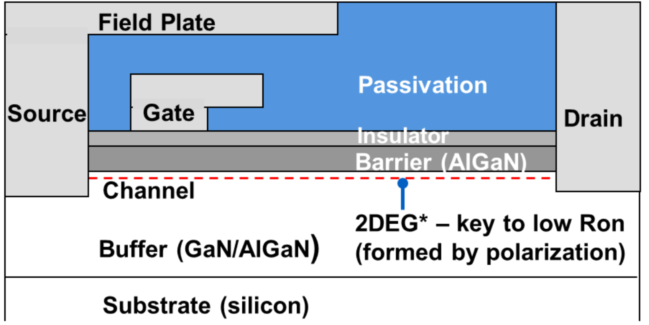
- 一、Why GaN and GaN HEMT?
- 二、GaN HEMT的发展历程和产业现状
- 三、GaN HEMT的特点及应用考虑
- 四、GaN HEMT的应用实例
- 五、小结

Why GaN and GaN HEMT?



AC-DC, DC-DC & DC-AC power electronics across many EEs

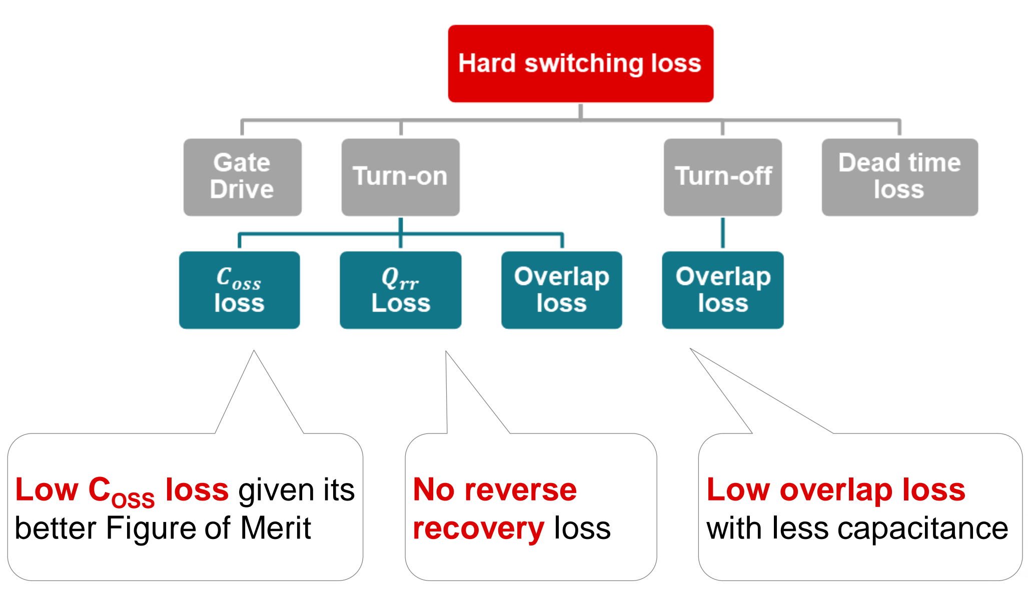
GaN Basics

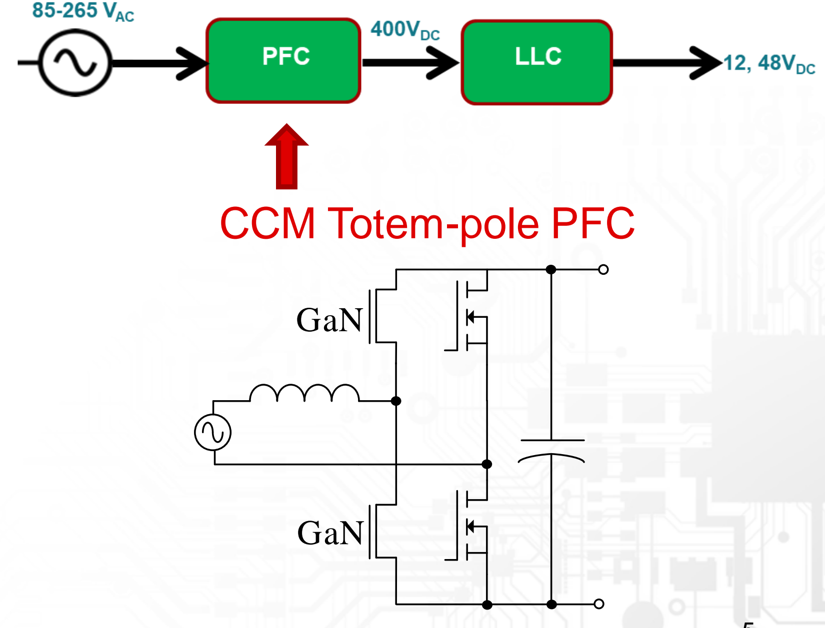


- The GaN FET is planar, vs. typical Si power FETs, which are vertical
- It is also called a HEMT, due to the High Electron Mobility channel or 2DEG
- The GaN layers are grown on a silicon substrate by MOCVD
- Field plates are used to optimize the E-field profile

Why GaN in hard-switching converters?

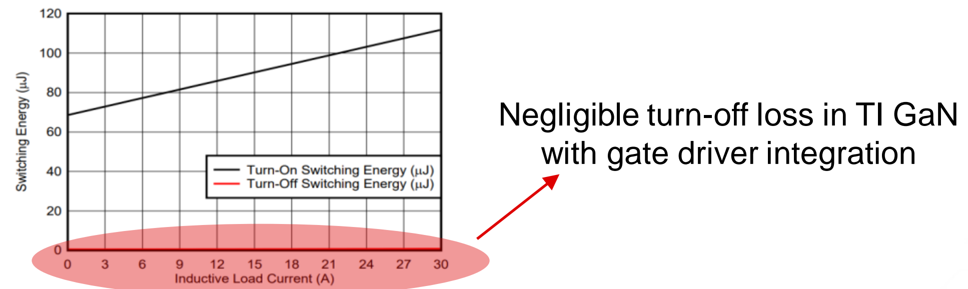
- **GaN Device Benefits**





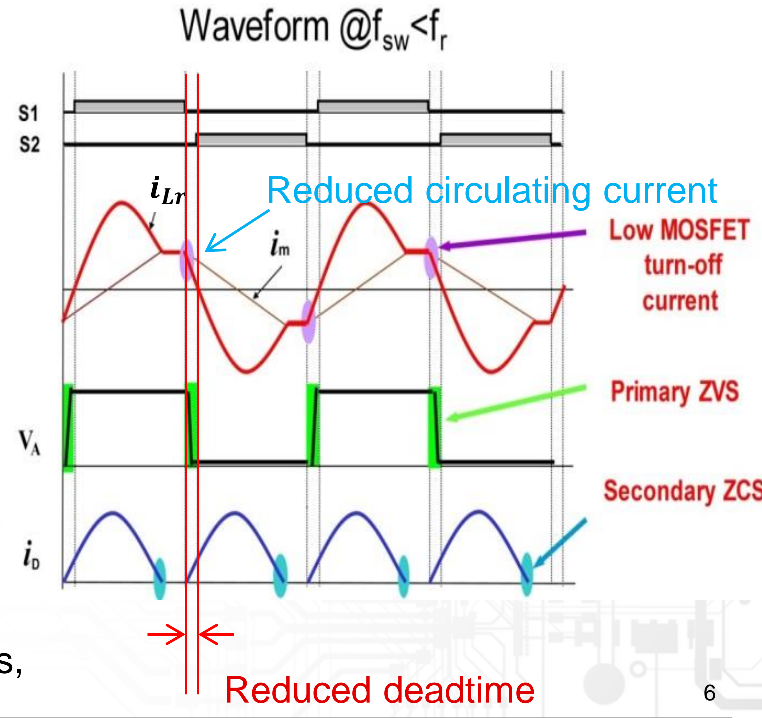
Why GaN in soft-switching converters?

- **Reduced output capacitance C_{OSS}**
  - Reduces dead-time
  - Low transformer magnetizing current to minimize circulating current loss & eddy loss.
- **Reduced turn-off overlap and gate driver losses**

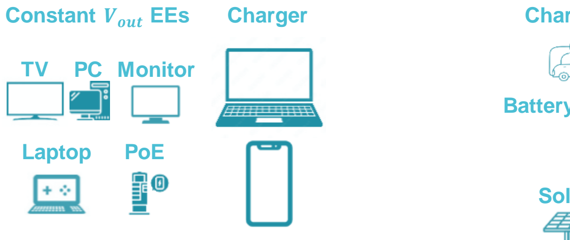


Negligible turn-off loss in TI GaN with gate driver integration

- **High power density in system**
  - GaN enables higher f_{sw} to reduce magnetic components, and enables magnetic integration.



GaN HEMT的发展历程和产业现状



Charger ESS
Battery Test System
Solar UPS

- GaN products covers EE applications widely
- GaN penetration is increasing in Automotive, Telecom & Infrastructure, Solar, and ESS
- GaN market is projected to reach $2.04 billion by 2028;

GaN HEMT的特点及应用考虑

- High critical **electric field** in GaN enables a lateral structure for high voltage application
- Due to the Piezoelectric Effect in GaN/AlGaN layer, a high **electron mobility** is achieved
- Much smaller **capacitance** is achieved in GaN with the lateral structure
- No **reverse recovery**
- Fast **switching speed**

Electric Field (MV/cm)
5
4
3
2
1
0
Si
SiC
GaN
Energy Bandgap (eV)
Thermal Conductivity (W/cm°C)
Electron Velocity (× 10^7cm/s)
Electron Mobility (cm^2/Vs)

Low on-resistance

Low switching loss

High Efficiency

High Frequency

High Power Density

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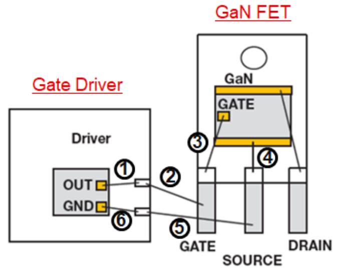
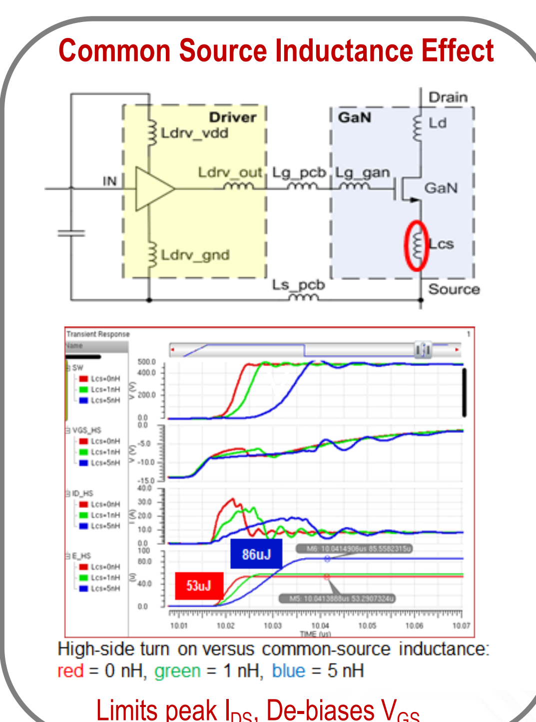
Gate driver layout affects switching loss

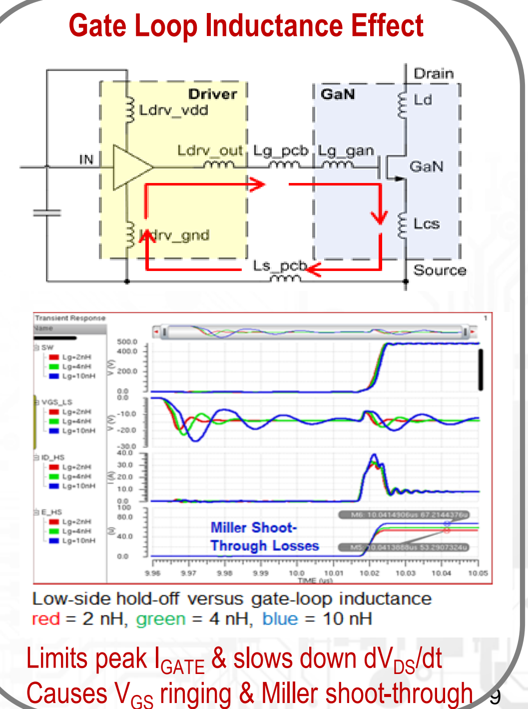


- **Common Source Inductance (CSI)**
  - Slows V_{DS} transitions.
  - Higher overlap losses (Hard-Switching).
  - Longer dead-times (Soft-Switching).
- **Gate Loop Inductance**
  - Limit peak gate current: slow down gate drive and induce high overlap losses in hard switching.
  - Gate overstress reliability risk.
  - Miller shoot-through risk.



High-side turn on versus common-source inductance: red = 0 nH, green = 1 nH, blue = 5 nH

Limits peak I_{DS}, De-biases V_{GS}



Low-side hold-off versus gate-loop inductance red = 2 nH, green = 4 nH, blue = 10 nH

Limits peak I_{GATE} & slows down dV_{DS}/dt
Causes V_{GS} ringing & Miller shoot-through

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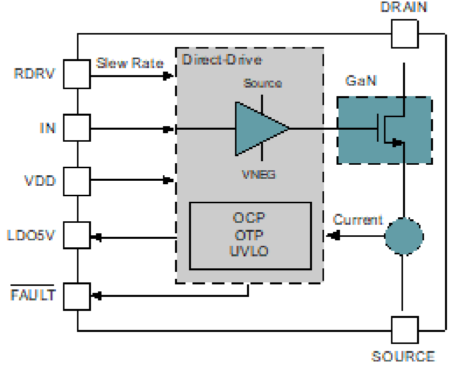
TI GaN Engineered for High-Frequency, Robustness



Integrated GaN FET, gate driver & more

- <1 nH common source inductance, <4 nH gate loop inductance
- on-chip V/I/T sensing, protections & reporting
- advanced power management features

+

Compact SMD package

- low parasitic lead inductance
- enhanced thermal management with top/bottom-side cooling

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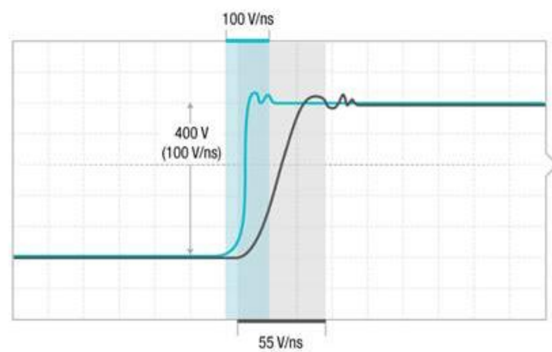
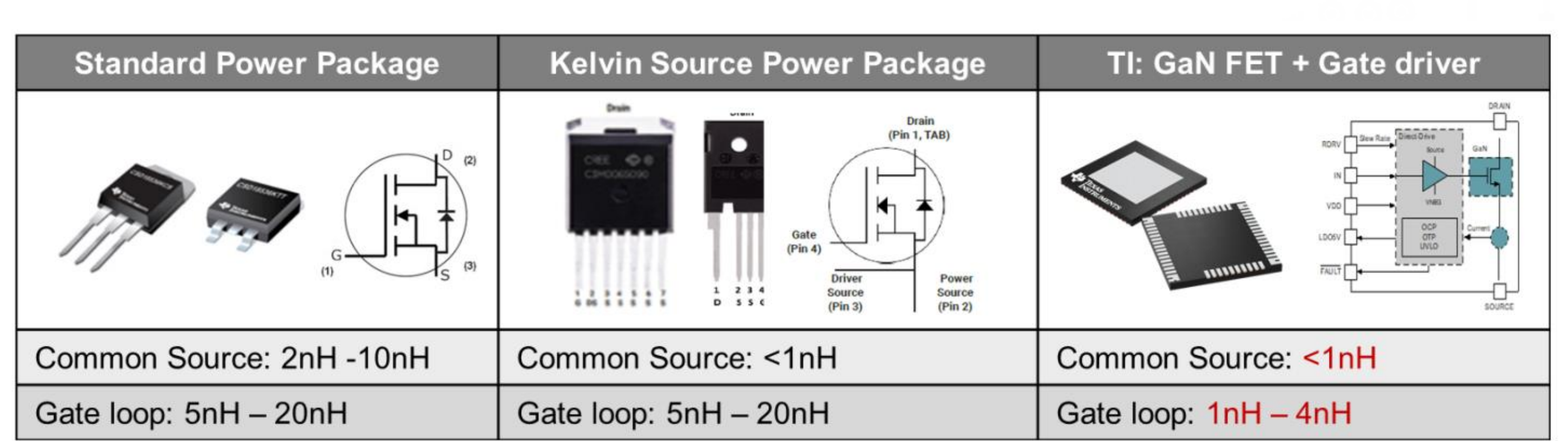


Design simplicity & confidence

- demonstrated dV_{DS}/dt capability of 150 V/ns
- dV_{DS}/dt adjustable between 30-150 V/ns for EMI vs efficiency
- compact PCB footprint

TI GaN engineered for high-frequency

- **SMD (QFN) multi-chip module package offers lowest parasitic inductance for high frequency operation.**



Standard Power Package	Kelvin Source Power Package	TI: GaN FET + Gate driver
Common Source: 2nH -10nH	Common Source: <1nH	Common Source: <1nH
Gate loop: 5nH – 20nH	Gate loop: 5nH – 20nH	Gate loop: 1nH – 4nH

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TI GaN Products

	Lower power (<500 W)		Higher power (>500 W)	
650-V half bridge	LMG2610 9 x 7 mm VQFN			
650-V/600-V FET	LMG3622 8 x 5.3 mm VQFN	LMG341xR050 8 x 8 mm VQFN	LMG3422R050 12 x 12 mm VQFN	LMG3422R030 12 x 12 mm VQFN
	LMG3624 8 x 5.3 mm VQFN	LMG341xR070 8 x 8 mm VQFN	LMG3522R050 12 x 12 mm VQFN	LMG352xR050/Q1 12 x 12 mm VQFN
	LMG3626 8 x 5.3 mm VQFN	LMG341xR150 8 x 8 mm VQFN		
≤ 100-V half bridge	LMG5200 8 x 6 mm QFM			
≤ 100-V			LMG2100R044 5.5 x 4.5 mm WQFN-FCRLF	

Legend: Top-Side Cooled (LMG2610, LMG3622, LMG3624, LMG3626, LMG341xR050, LMG341xR070, LMG341xR150, LMG3422R050, LMG3422R030, LMG5200); Bottom-Side Cooled (LMG3522R050, LMG352xR050/Q1, LMG2100R044)

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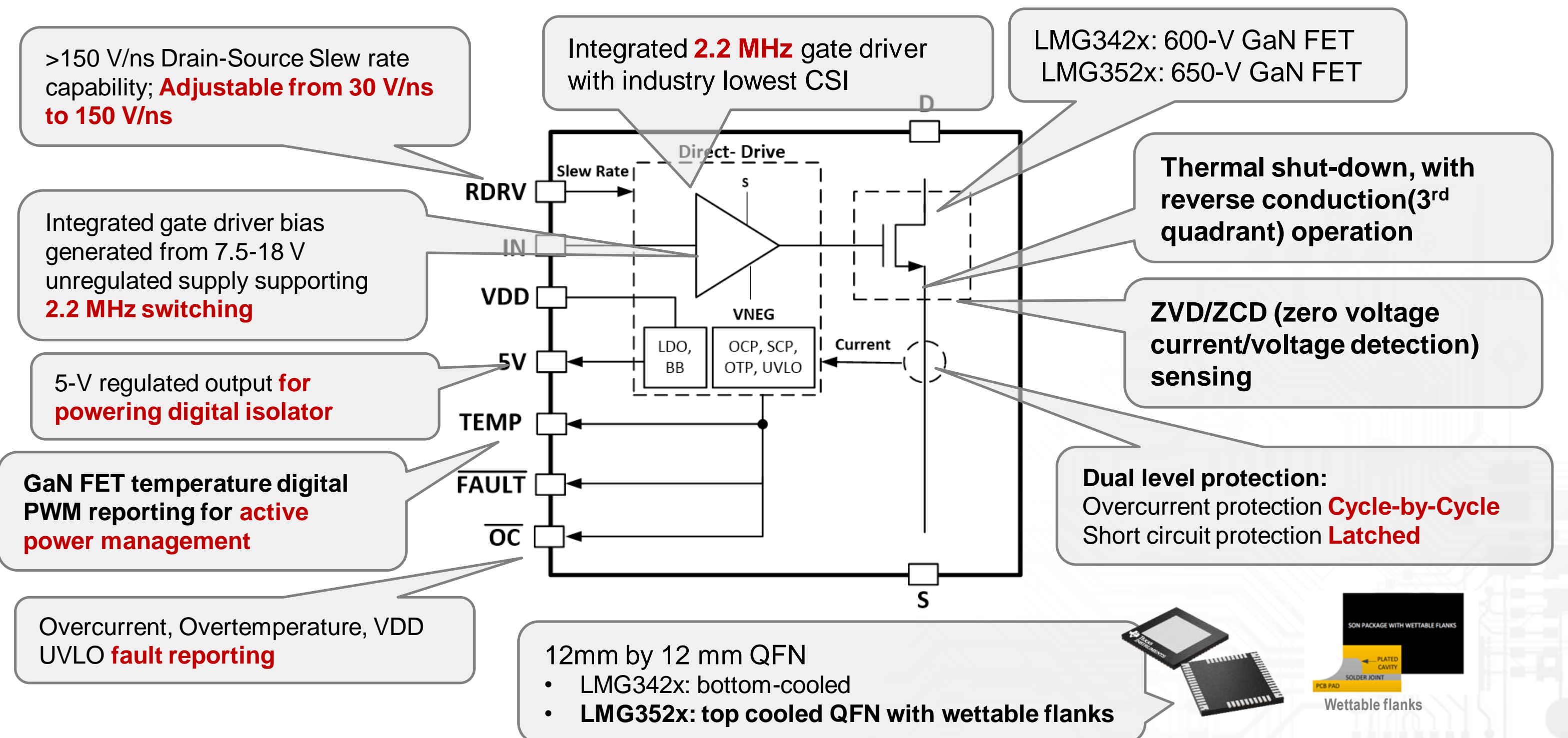
LMG342x/352x: TI Gen II GaN Features



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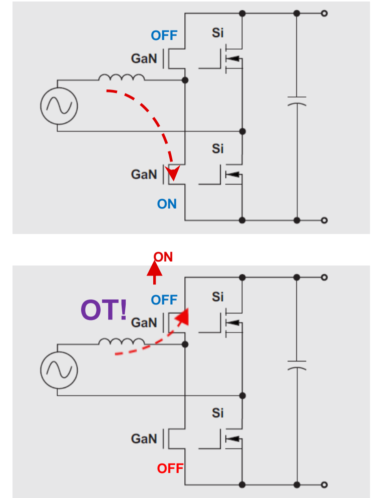
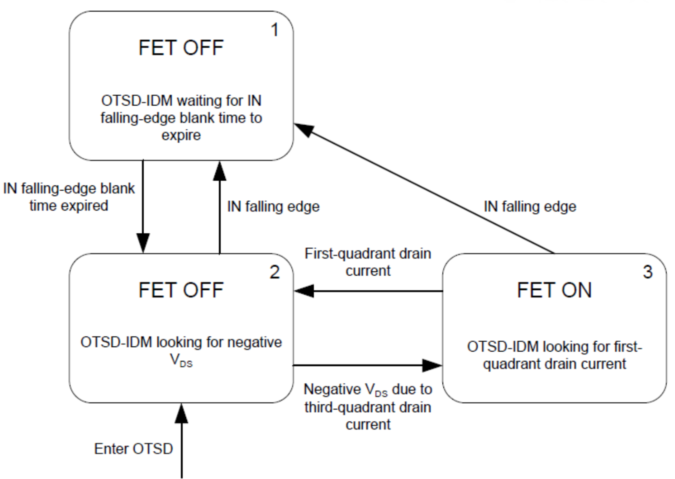
Robustness Highlight 1: Over Thermal Shutdown – Ideal Diode Mode in AC Drop Test for PFC

- **OTSD-IDM**
  - When over thermal event is triggered: the FET will be automatically turned on when it detects the 3-rd quadrant current.





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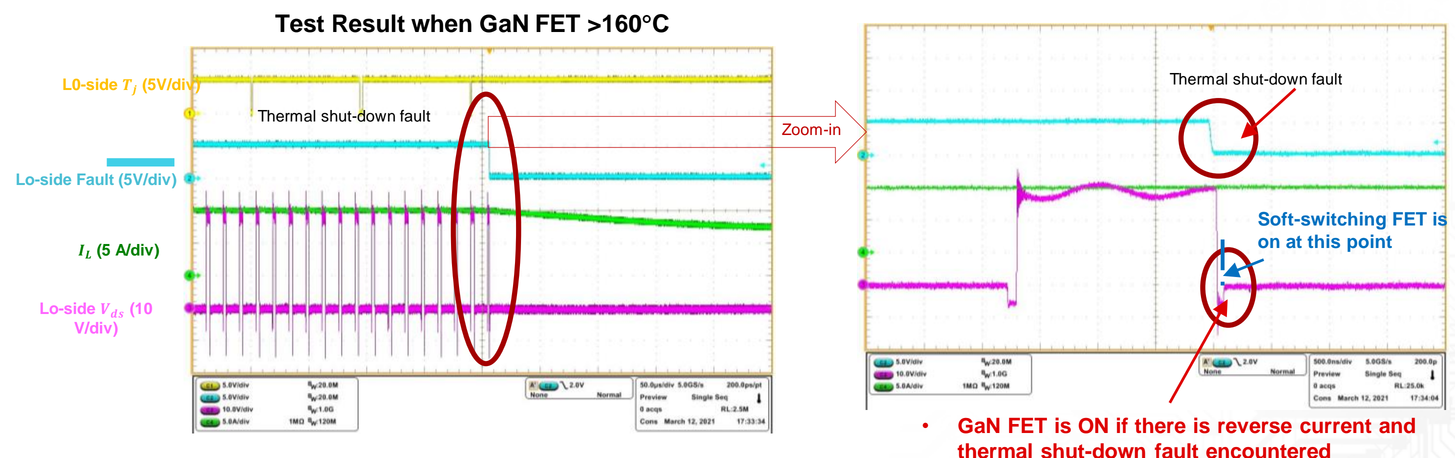
Robustness Highlight 1: Over Thermal Shutdown – Ideal Diode Mode in AC Drop Test for PFC

- LMG342X/352XR0X0 is turned ON when a reverse current is flowing from source to drain and thermal shut-down is encountered
- This behavior mitigates risk for thermal run-away and device failure



- GaN FET is ON if there is reverse current and thermal shut-down fault encountered
- Voltage drop reduced to = I_{SD}*30mΩ

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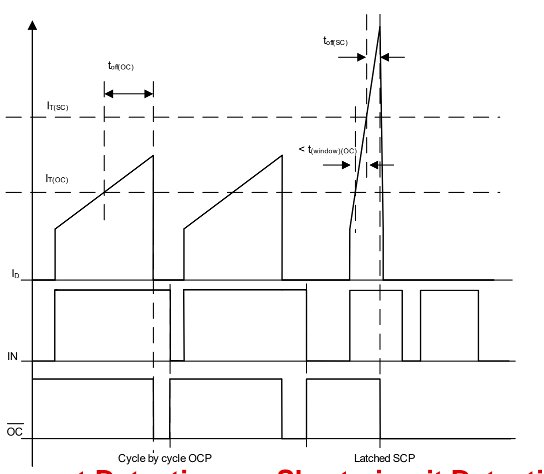
Robustness Highlight 2: Short Circuit Protection (SCP)

- Abnormal short circuit conditions are latched off for system intervention
- dI/dt used to differentiate between OCP & SCP modes

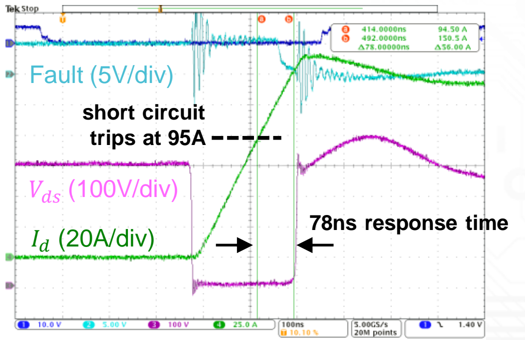
LMG342x/352x	50mΩ	30mΩ	Action
Over-Current Protection*	50A	70A	Cycle-by-Cycle
Short-Circuit Protection*	**75A**	**95A**	**Latched-off**

* Typical Values

[schedule, specs, features & pinouts subject to change without prior notice.]



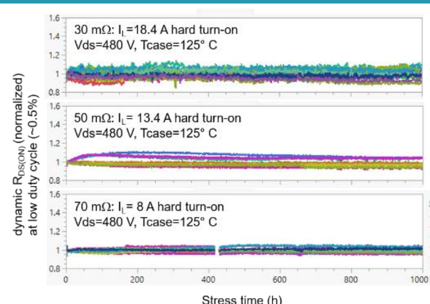
Over-current Detection vs. Short-circuit Detection



Short Circuit Test at 400V

Robustness Highlight 3: TI GaN Qualification & Reliability Summary

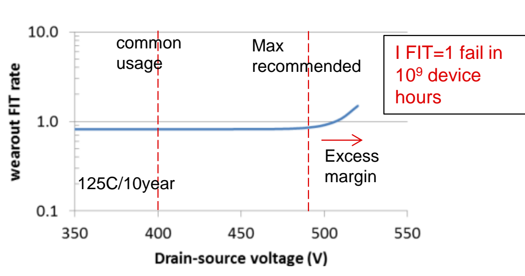
Reliable in Power Supply



- JESD47/AECQ100 device qualification
- Every GaN product qualified inside power supply running at high voltage/current /temp against *charge trapping*

Dynamic Rdson

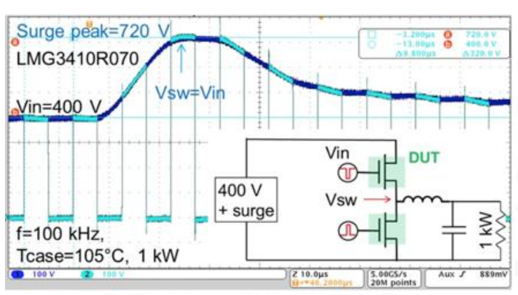
Intrinsically Reliable GaN



- <1 FIT over 10-years at 125C, from 1.8Mhours of reliability test data for *time dependent breakdown*
- Over 1 billion years switching lifetime under hard-switching against *hot-electron wear-out*

Lifetime

Robust by Design



- Designed to withstand 720V voltage surge
- Integrated over-current and over-temperature protection for every GaN FET

No avalanche? No problem!

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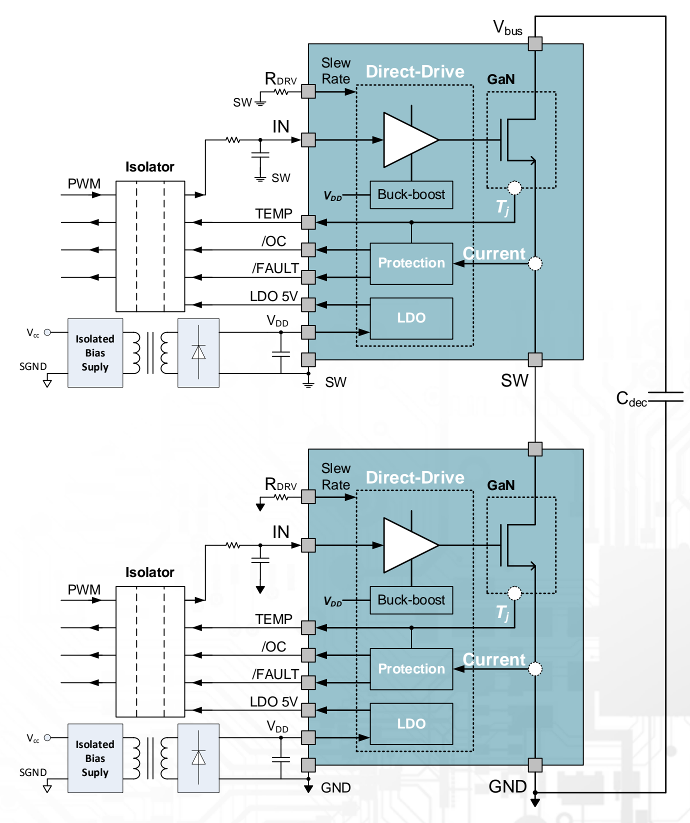
Power Stage Design

- **Parasitics**
  - Inductance
    - Power Loop
  - Capacitance
    - Switching node
- **Noise Coupling**
  - Isolator/iso bias/PCB/heatsink
- **Thermal Design**
  - Top/Bottom Cooling
  - Heatsink/TIM



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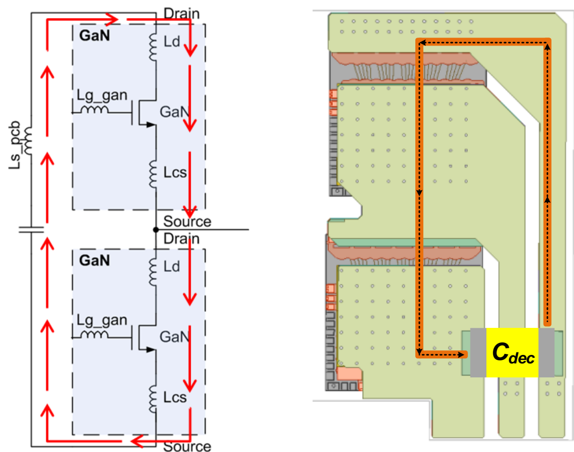
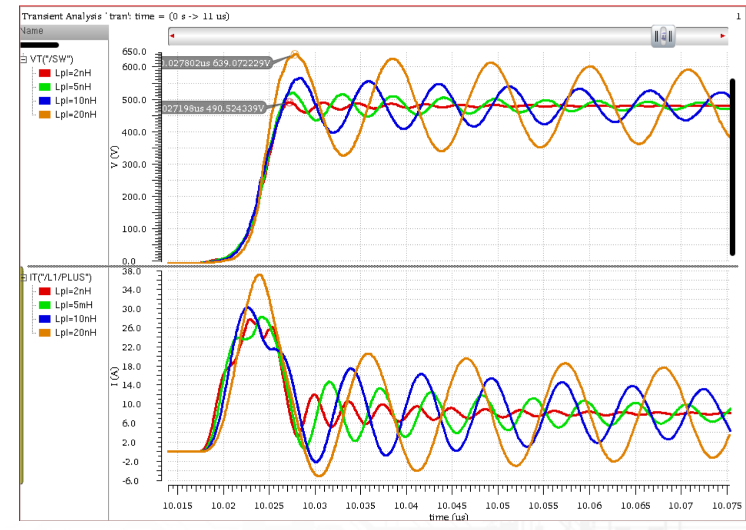
Why power loop layout is critical?

- **Large Power Loop Inductance will**
  - Increase ringing and cause EMI concerns
  - Increase voltage spikes
  - Induce noises causing signal integrity issue





V_{sw} ringing versus power loop inductance

red = 2nH, green = 5nH, blue = 10nH, orange = 20nH

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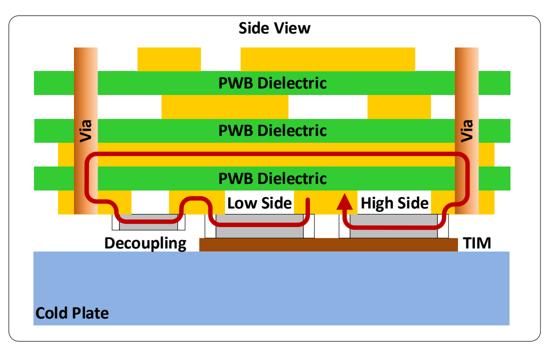
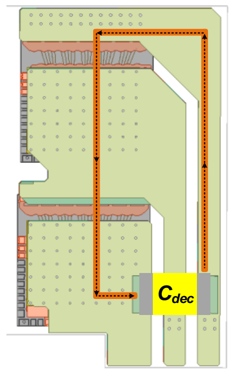
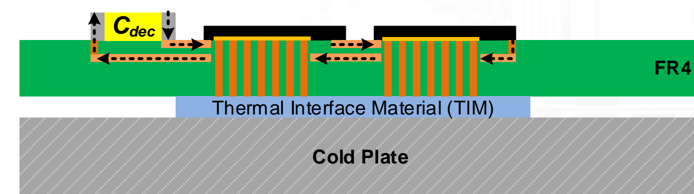
Good practice for power loop layout

- **Good Practice Procedures**
  - Place GaN devices and decoupling capacitors close together.
  - Use multiple ceramic decoupling capacitors with low-inductance.
  - Vertical loop: use wide return path in the adjacent layer for inductance cancellation.





L_{ds} = 12.7 nH



L_{ds} = 2.0 nH

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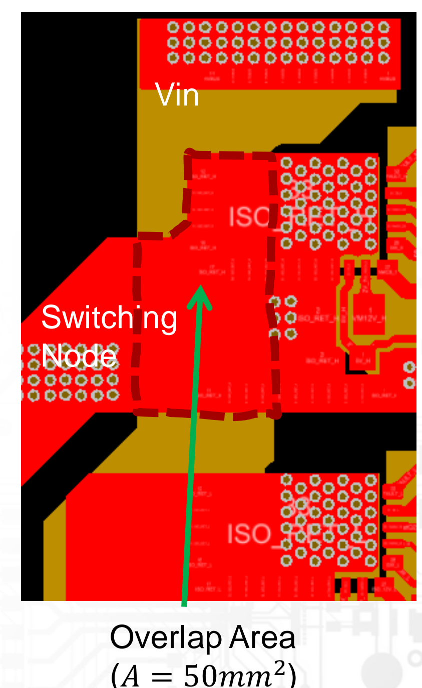
Parasitic Capacitance in Layout

- **Potential Problem**
  - GaN has small output capacitance. For example LMG3410R150 has only 68pF.
  - A bad layout of $150mm^2$ of switch node and ground overlap area can result in 51pF of additional switch node capacitance
- **Solution**
  - Minimize switch node overlap area.
  - A good layout of $50mm^2$ only results in 17pF of added capacitance



Overlap Area
$(A = 50mm^2)$

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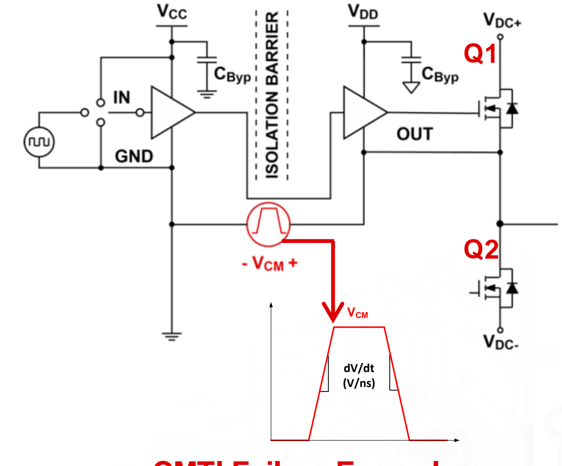
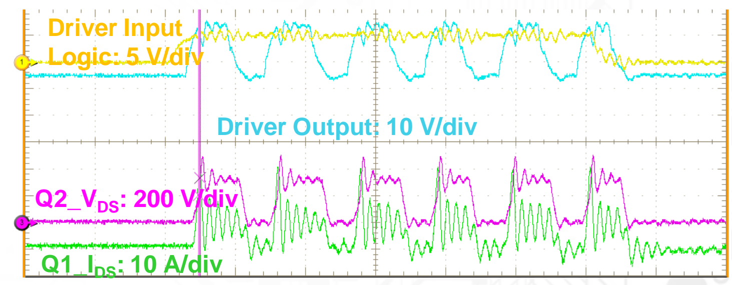
Noise Coupling

- High dv/dt switching can lead to common mode noise.
- Without good common mode transient immunity (CMTI), parasitic noise currents could cause malfunction of the driver
  - Missing pulse
  - Excessive propagation delay
  - High or low error
  - Output latch



CMTI Failure Example



Time: 100 ns/div

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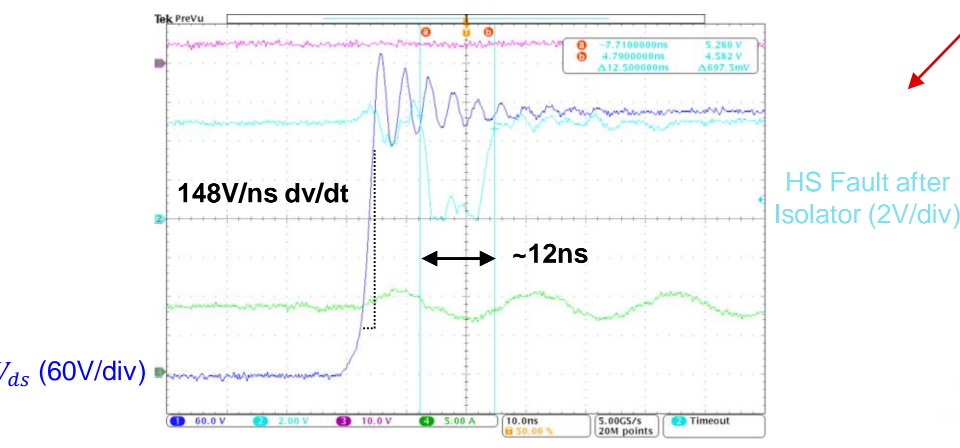
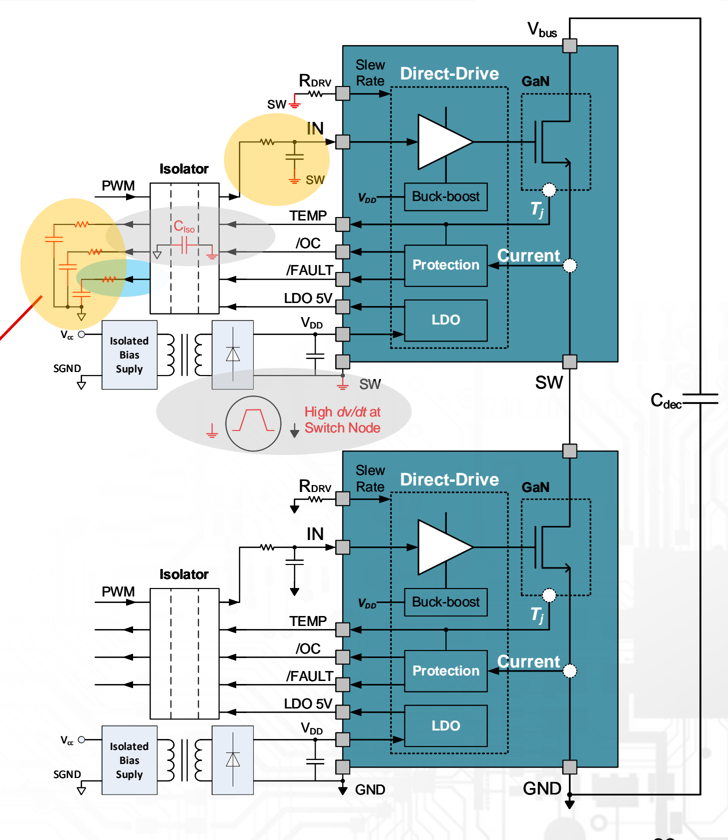
Noise Coupling through Isolator

- The isolator's insufficient CMTI is causing the glitch at isolator output.
- **Solutions:**
  - Choose higher CMTI isolator
  - Isolator with default low output is preferred
  - An RC filter is recommend on the **high-side isolator's output**





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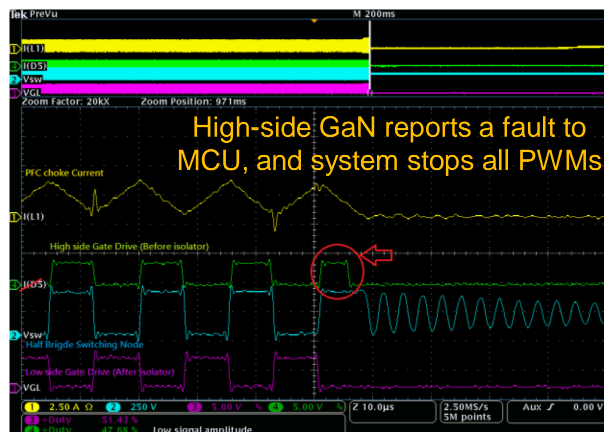
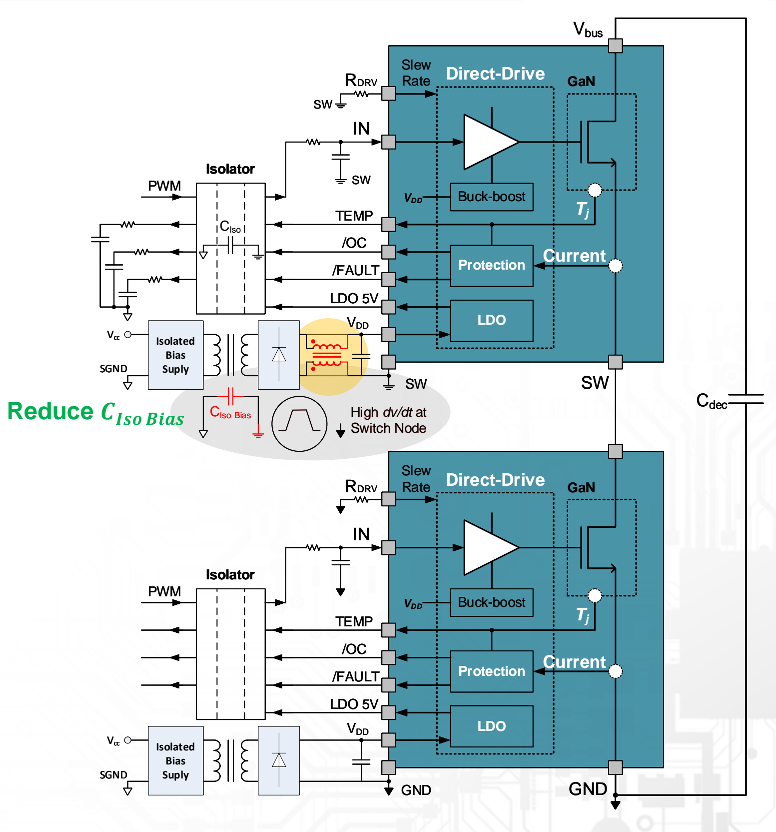
Noise Coupling through Iso-Bias

- Large $C_{Iso\ Bias}$ induces common-mode noise to signal ground and affects signals like fault feedback or PWMs.
- **Solutions:**
  - Low coupling capacitance in the transformer and PCB layout.
  - Add common mode choke.



system stops switching at high dv/dt



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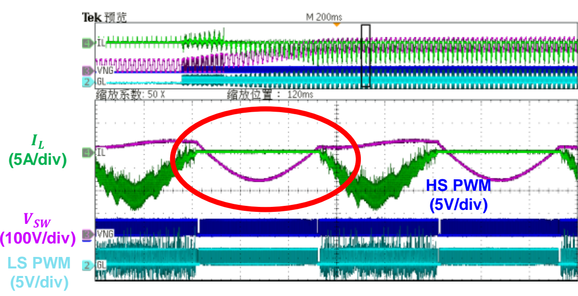
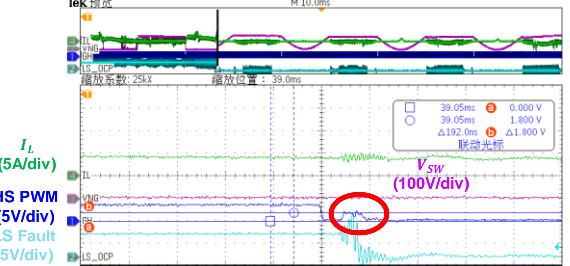
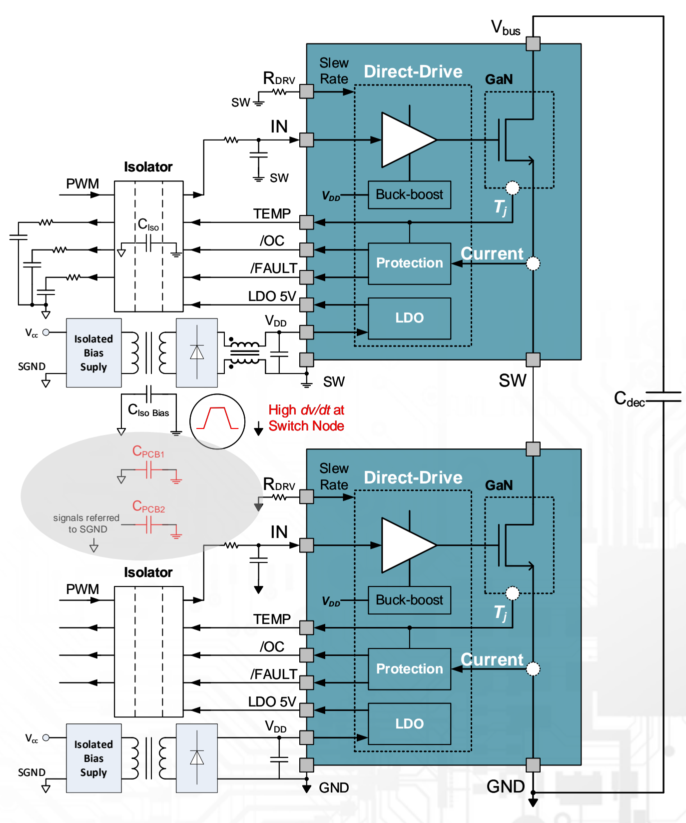
Noise Coupling through PCB

- Root cause: the switch node has overlap with the **control ground** and signals leading to capacitive coupling noises.







- No current in positive AC cycle
- LS GaN triggered fault

- When LS GaN is turning on, HS PWM has a 1.8V noise causing shoot-through.

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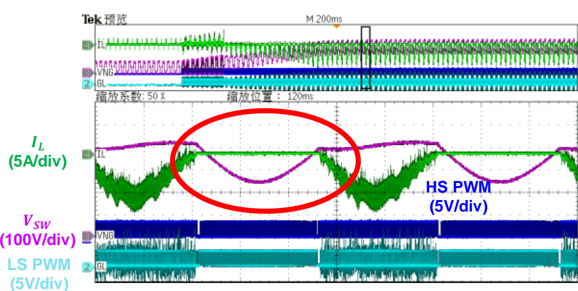
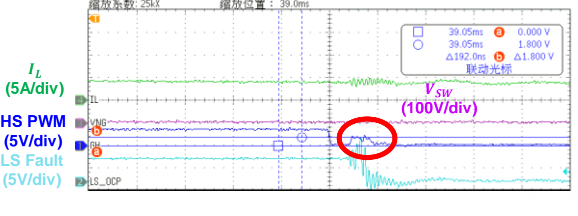
Check switch node coupling

- Root cause: the switch node has overlap with the **control ground** and signals leading to capacitive coupling noises.
- **Solution:** avoid signal tracing above or below the switch node plane unless the signals are referring to switch-node.





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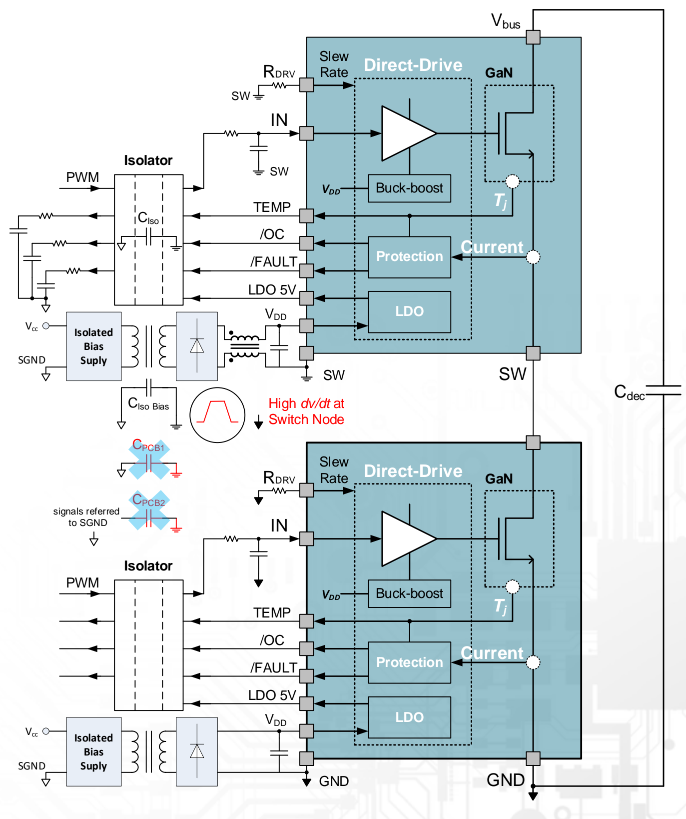

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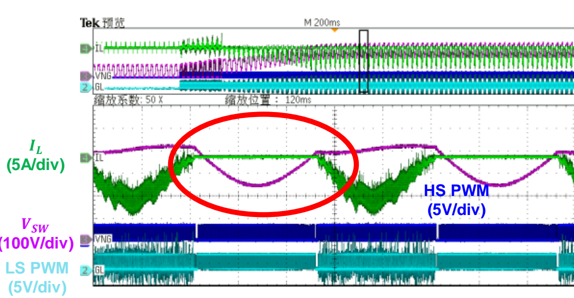
Check switch node coupling

- Root cause: the switch node has overlap with the **control ground** and signals leading to capacitive coupling noises.
- **Solution:** avoid signal tracing above or below the switch node plan unless the signals are referring to switch-node.



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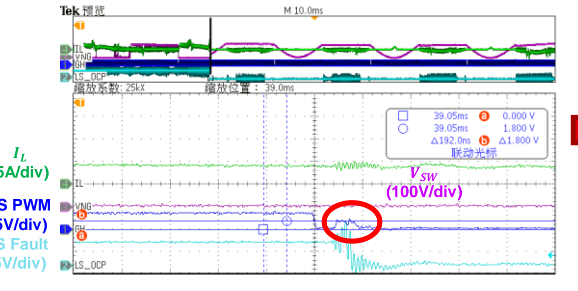

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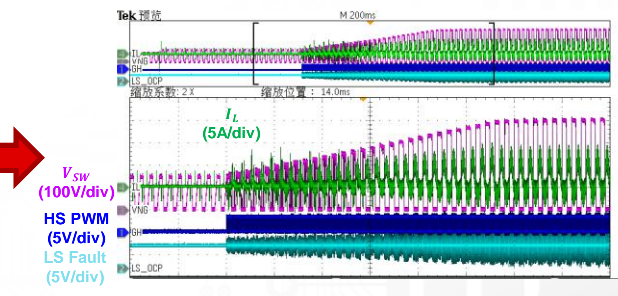
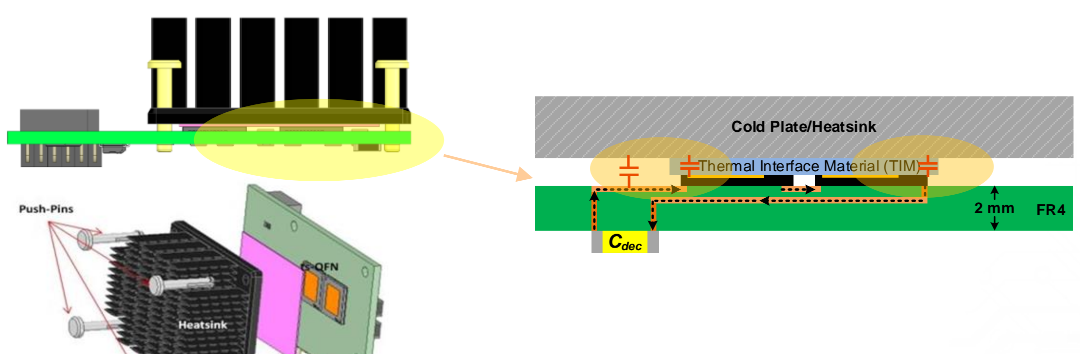
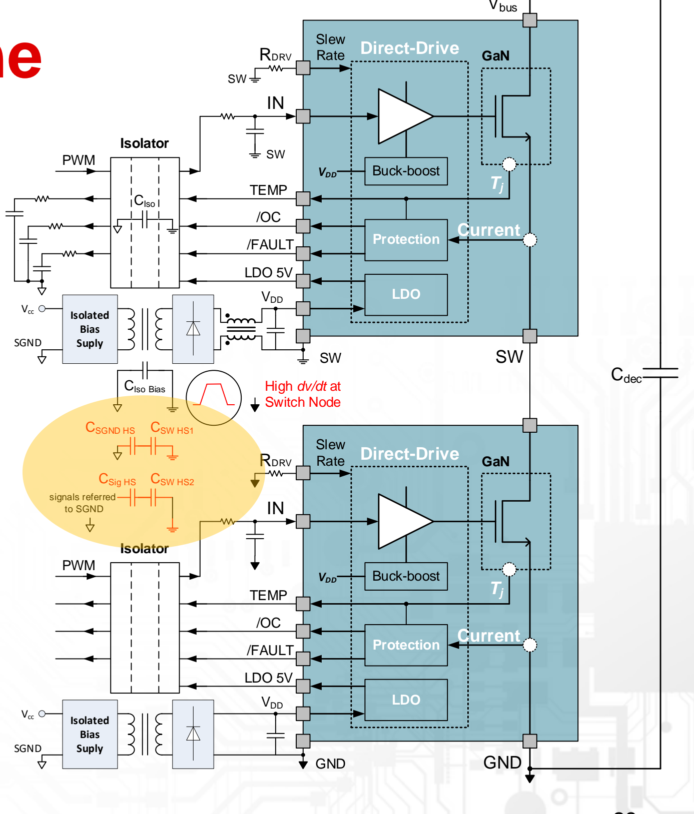


- Rework the board and remove the noise coupling from switch node.
- Modified their layout and solved the problem.

Noise Coupling through Cooling Plane

- **Noise coupling through cooling:**
  - Most GaN devices' exposed thermal pad is electrically connected to device's drain or source.
  - Capacitive coupling exists between the switch-node and signal ground or signals.





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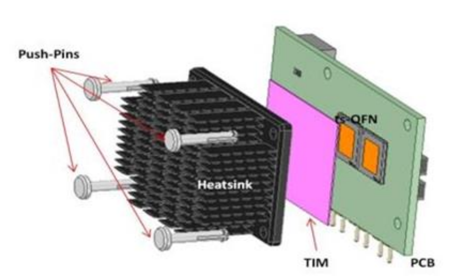
Ways to reduce noise coupling to cooling plane

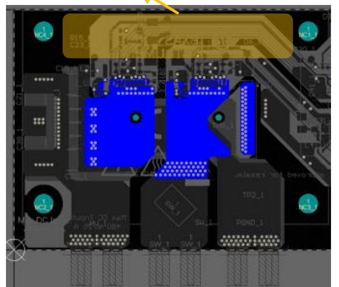
- Minimize the **traces** and **vias** in adjacent layers to cooling plane.
- Increase distance to cooling plane in certain area to reduce coupling capacitance.

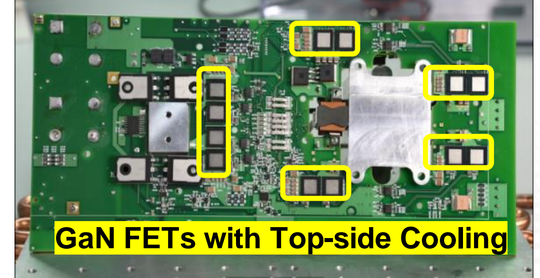
$$C = \frac{\varepsilon \cdot A}{\boldsymbol{d}}$$

GaN FETs
PWB
Cold Plate
Thermal Interface Material (TIM)

most traces in inner layers

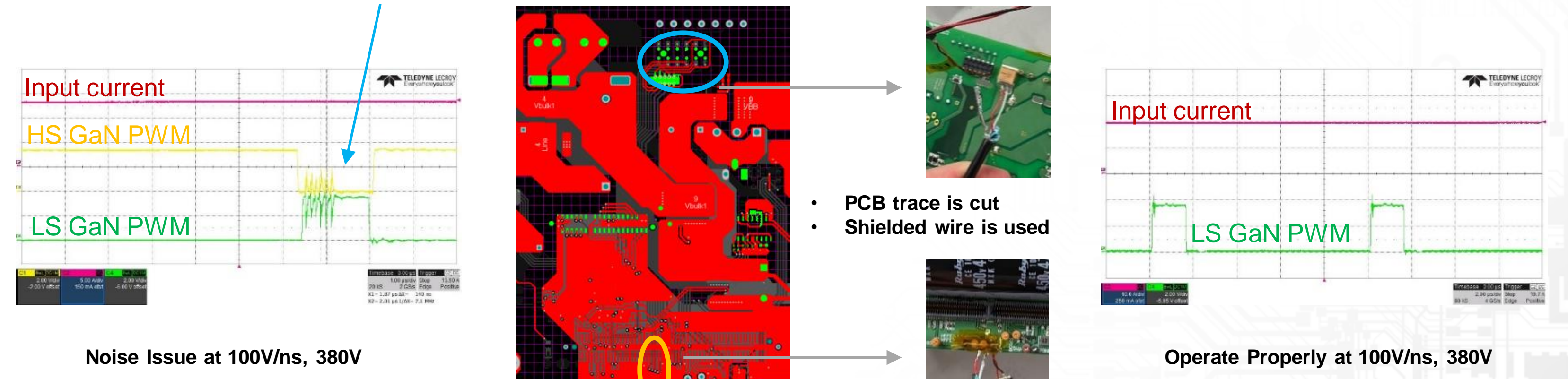






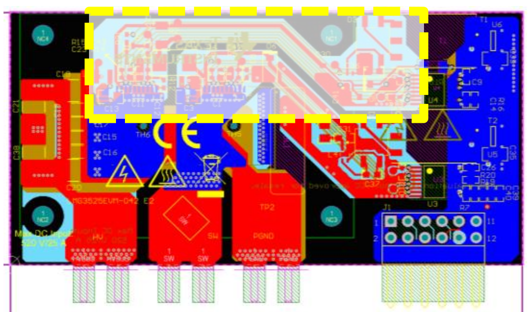
Noisy PWM Signals

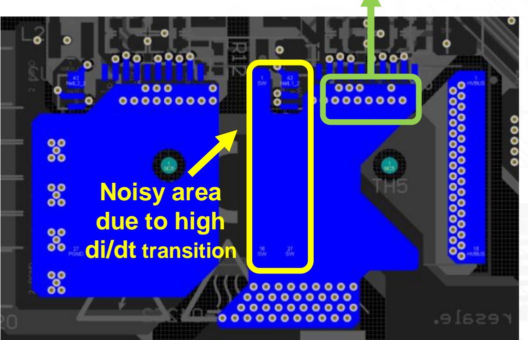
- **PWM signals from the controller have large noises at high *dv/dt* operations**



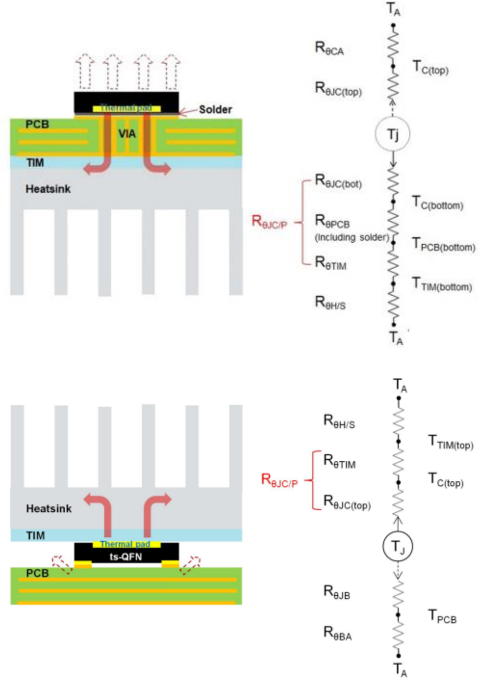
Good practices to maintain signals integrity

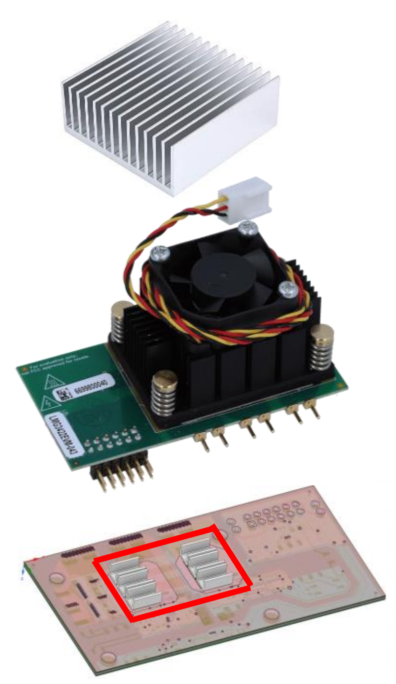
- **Signal Shielding:** all signals need to be shielded by its reference ground. Shielding is recommended for both the controller's outputs and the isolator outputs.
- **Kelvin Signal Connection:**
  - Avoid the noise area where high transient power passes through due to PCB trace impedance.
  - The quiet area with significantly less power transition is used for signal ground.



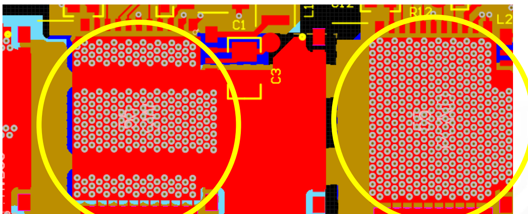


Thermal Design

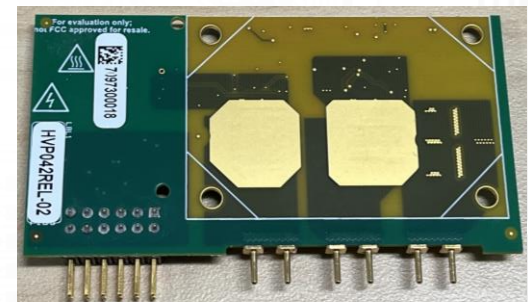




- Thermal via pattern



- Via filled and plated



List of Thermal Interface Materials (Pad)

TIM Part #	Manufacturer	Thermal Conductivity (W/mK) on datasheet	Dielectric Strength (kV/mm)	Thickness (mm)
HD90000	Fujipoly	7.5	N/A	0.9 (after compression from nominal 1mm)
GR80A	Fujipoly	8	8	
XLIM-HL	Sekisui	10	N/A	
GR130A	Fujipoly	13	7	
T-Work9000	LiPoly	20	8	
EI-20	Thermexit	20	7.8	

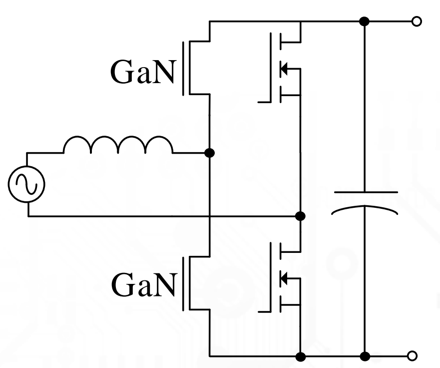
Methods of Thermal Improvement

- **Reduce power loss**
  - Reduce dead time, switching frequency etc
  - Switch to lower $R_{ds,on}$ if conduction loss dominates, or switch to higher $R_{ds,on}$ if switching loss dominates
- **Reduce $R_{th\text{-}ja}$**
  - Select higher thermal conductivity TIM
  - Increase air speed
  - Increase # of thermal vias if bottom cooled device
  - Increase fin height in heatsink
  - Change from Al to Cu heatsink
  - Increase distance between GaN and other power loss components

GaN HEMT的应用实例

- Po = 1.8kW @ 180V, 1kW @ 90V
- fsw = 65kHz, Ta = 65°C, Air flow speed = 10m/s
- Topology: CCM totem pole PFC

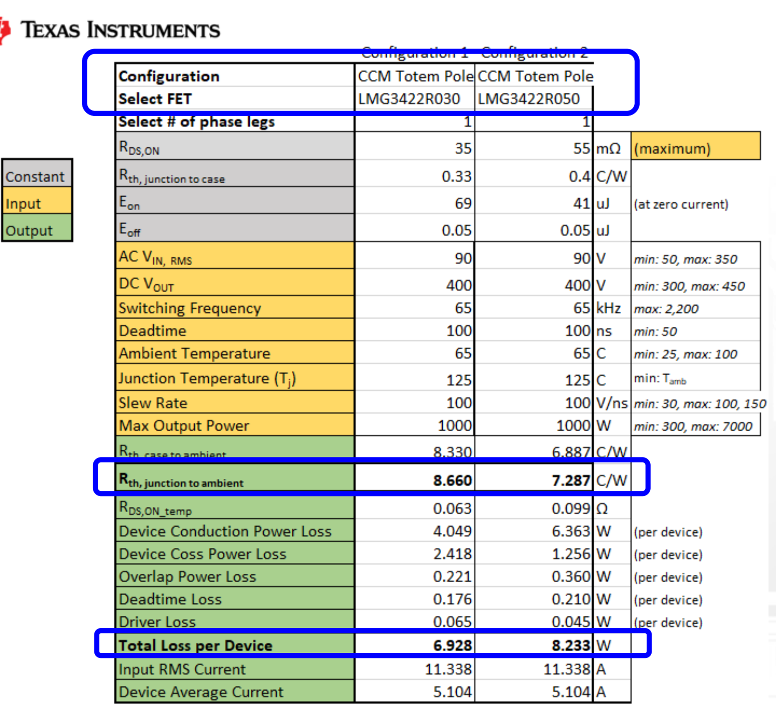
CCM Totem-pole PFC



- Device selection
- Heatsink selection

Step 1: Select the proper TI GaN FET

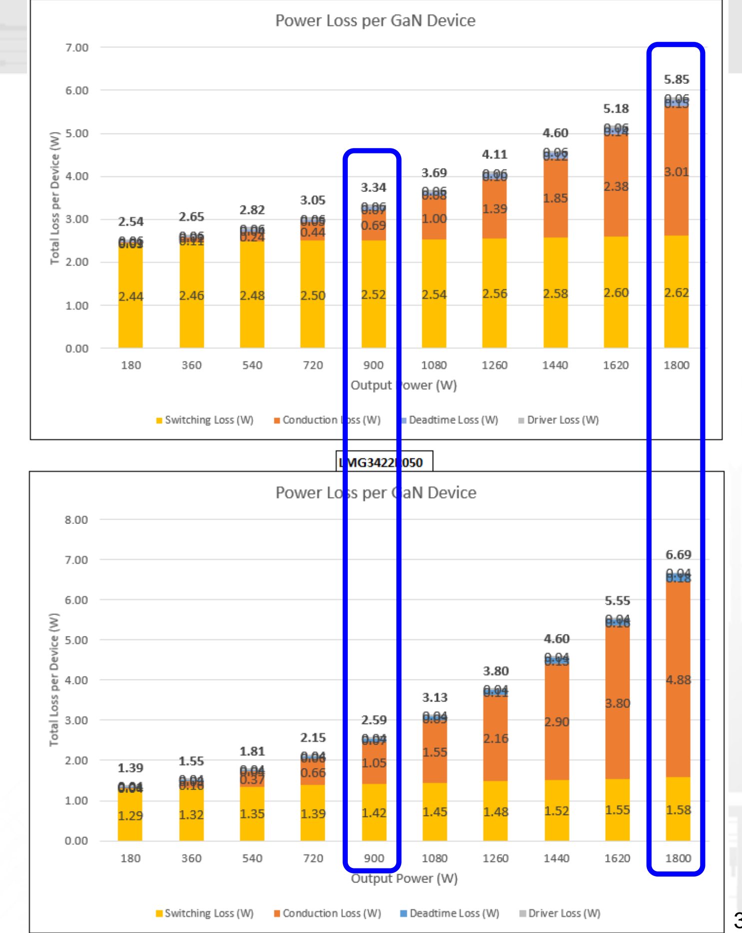
- TI provides Power Loss Calculator XLS tools for CCM Totem Pole PFC Power Loss Calculation Excel Sheet
- In XLS tool, use the two configurations to compare different FETs for power losses and junction temperature
- It is important to select the right on-resistance (R_{ds}) FET based on its power loss (for efficiency, thermals)
- Once the optimal FET is chosen, move to thermal design



	Configuration 1	Configuration 2		
Configuration	CCM Totem Pole	CCM Totem Pole		
Select FET	LMG3422R030	LMG3422R050		
Select # of phase legs	1	1		
$R_{DS,ON}$	35	55	mΩ	(maximum)
$R_{th, junction\ to\ case}$	0.33	0.4	C/W	
E_{on}	69	41	uJ	(at zero current)
E_{off}	0.05	0.05	uJ	
AC $V_{IN,\ RMS}$	90	90	V	*min: 50, max: 350*
DC V_{OUT}	400	400	V	*min: 300, max: 450*
Switching Frequency	65	65	kHz	*max: 2,200*
Deadtime	100	100	ns	*min: 50*
Ambient Temperature	65	65	C	*min: 25, max: 100*
Junction Temperature (T_j)	125	125	C	min: T_{amb}
Slew Rate	100	100	V/ns	*min: 30, max: 100, 150*
Max Output Power	1000	1000	W	*min: 300, max: 7000*
$R_{th, case\ to\ ambient}$	8.330	6.887	C/W	
$R_{th, junction\ to\ ambient}$	**8.660**	**7.287**	C/W	
R_{DS,ON_temp}	0.063	0.099	Ω	
Device Conduction Power Loss	4.049	6.363	W	(per device)
Device Coss Power Loss	2.418	1.256	W	(per device)
Overlap Power Loss	0.221	0.360	W	(per device)
Deadtime Loss	0.176	0.210	W	(per device)
Driver Loss	0.065	0.045	W	(per device)
Total Loss per Device	**6.928**	**8.233**	W	
Input RMS Current	11.338	11.338	A	
Device Average Current	5.104	5.104	A	

FET Selection Tradeoffs

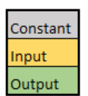
- Consider the trade-offs when selecting the FET
- Lower R_{ds} FET has lower conduction losses but higher switching losses
- The power losses between two FETs can be different at different load conditions, which depends on power level, switching frequency etc, the main reason is related to the proportion of conduction & switching losses
- In server/datacenter/telecom applications,
  - 50% load efficiency and nominal AC is the key spec so select FET based on this first.
  - But the thermal design of the chosen FET must support worst operating conditions, the max power at min Vin and max Ta.
  - If the thermal challenge is too difficult to solve, then choose a lower R_{ds} FET



Thermal Check

- Target $R_{th\text{-}ja}$ = 7.2°C/W
- Solderable heatsink is achievable

- Select LMG3422R050
- Solderable heatsink



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Total Loss per Device	**6.928**	**8.233**	W	
Input RMS Current	11.338	11.338	A	
Device Average Current	5.104	5.104	A	

GaN HEMT的应用实例 – 3.6kW 1-ph totem-pole PFC stage

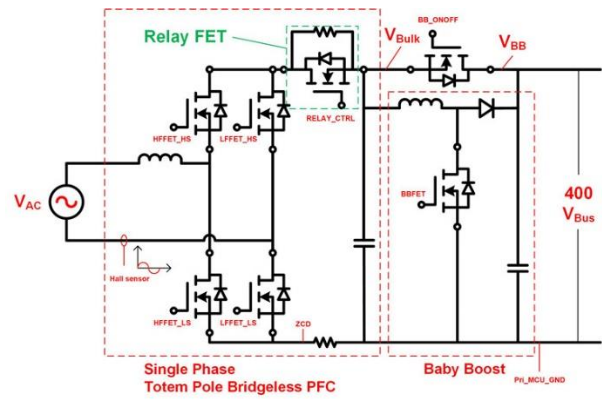
Design Features

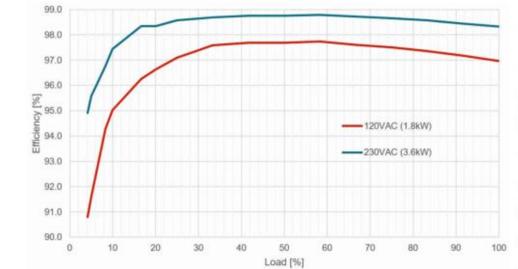
- 230V AC input AC/DC stage of a >110W/in³ PSU for server/telecom
- PFC operates at 65kHz using only **2x 30mOhm GaN in** top-side cooled package and **1x C2000** controller (F28002x / F28004x)
- **Baby boost architecture** allows for smaller hold up cap, higher density, and AC line drop out
- **Relay FET** can be smaller than traditional solution saving space on the board and increasing density

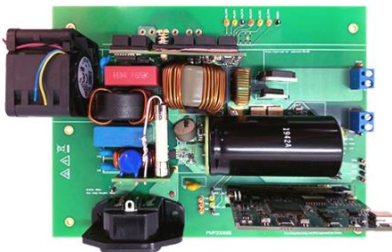
Design Benefits

- **> 180-W/in³ power density** AC/DC stage
- **Reduced size of heatsink and bulk capacitor**
- Partners with other HV-LV DC/DC reference designs

PFC specification	Value
Nominal AC Input	230Vac
DC link voltage	400Vdc ± 10V
Maximum Power	3.6kW (4.5kW surge)
Efficiency w/o Fan losses	98.7% @50% load, 92% @100% load
Dimension	38mm x 68mm x 175mm







Texas Instruments

Thank you